

Form PTO 1449 (Rev. 2-32)		U.S. Department of Commerce Patent and Trademark Office		Atty. Docket No. IMPJ-0003D1		Serial No.: 10/661,037	
Information Disclosure Statement by Applicant				Applicant: John D. Hyde et al.			
(Use several sheets if necessary)				Filed: September 12, 2003 Group: 2822			
U.S. Patent Documents							
Init.		Document No.	Date	Name	Class	Subclass	Filing Date
me	AS	6,222,771	4/24/2001	Tang et al.	365	185.22	
	AT	6,452,835	9/17/2002	Diorio et al.	365	185.03	
	AU	6,479,863	11/12/2002	Caywood	257	321	
	AV	6,534,816	5/18/2003	Caywood	257	314	
<div style="border: 1px solid black; height: 100px; width: 100%;"></div>							
Foreign Documents							
Init.		Document No.	Date	Country	Class	Subclass	Translation Yes No
<div style="border: 1px solid black; height: 100px; width: 100%;"></div>							
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
me	AW	Hyde, et al.; "A Floating-Gate Trimmed, 14-Bit, 250 Ms/s Digital-to-Analog Converter in Standard 0.25 um CMOS", Impinj, 2002 Symposium on VLSI Circuits, Honolulu HI; pp 328-331.					
<div style="border: 1px solid black; height: 100px; width: 100%;"></div>							
Examiner					Date Considered		
[Signature]					6/24/03		
Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.							